What is claimed is:

1. An apparatus comprising:

a host;

a plurality of cards connected to said host, each of said cards operating within an independent operating voltage range; and

a voltage negotiator for determining a common operating voltage range, said common operating voltage range is a common denominator of all independent operating voltage ranges of all of said cards,

wherein said host communicates with said cards within said common operating voltage range.

2. The apparatus according to claim 1, wherein said voltage negotiator is located in said host.

3. The apparatus according to claim 1, wherein each of said cards simultaneously provides the corresponding operating voltage range to said host.

4. The apparatus according to claim 3, each of said cards further comprises a plurality of data bits, said plurality of data bits representing the operating voltage range of the corresponding card.

5. The apparatus according to claim 4, wherein each of said cards provides the corresponding data bits to said host representing the operating voltage range.

6. The apparatus according to claim 5, wherein said voltage negotiator comprises a plurality of Wired-or gates, each of said wired-or gates connected in parallel with each of the cards.

7. The apparatus according to claim 6, wherein said common operating voltage is represented by a plurality of data bits located inside the host.

8. The apparatus according to claim 1, wherein at least one of said card is a memory card.

9. The apparatus according to claim 1, wherein at least one of said card is an interface card.

10. In a memory system comprising a host, a plurality of cards connected to said host, wherein data is transferred between said cards and said host, a method of determining a common operating voltage range for operating said memory system, comprising:

each of said cards providing an independent operating voltage range to said host; and

finding a common denominator of said independent operating voltage ranges provided by said cards, said common denominator is the common voltage range.

11. The method according to claim 10, wherein the independent operating voltage ranges are simultaneously provided to said host by said cards.

12. The method according to claim 11, wherein said independent operating voltage ranges are stored in a plurality of data bits in the corresponding cards.

13. The method according to claim 12, said finding step comprises:

wiring AND all the independent operating voltage ranges provided by said cards.

14. The method according to claim 13, said host comprising a plurality of data bits for storing said common operating range.

15. The method according to claim 10, wherein at least one of said cards is a storage device.

16. The method according to claim 10, wherein at least one of said cards is an interface device.

17. A memory system comprising:

a plurality of memory groups, each of said memory groups comprising a plurality of memory sectors, each of said memory sectors comprising a plurality of memory cells;

a plurality of group tags, each of said group tags corresponds to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are erasable; and

a plurality of sector tags, each of said sector tags corresponds to a memory sector, each of said sector tags indicating whether the memory cells under the corresponding memory sector are erasable,

wherein all the memory cells belonging to one memory sector are erasable when either the corresponding sector tag or the corresponding group tag of the memory sector is set;

wherein any combination of memory sectors in a memory group can be simultaneously erased, and any combination of the memory groups can be simultaneously erased.

18. The memory system according to Claim 17, wherein the number of memory sectors in each memory group is configurable.

19. The memory system according to Claim 18, wherein the corresponding sectors in each memory group is calculated in real time.

20. The memory system according to Claim 17, wherein the number of memory cells in each memory sector is configurable.

21. The memory system according to Claim 20, wherein the corresponding memory cells in each memory sector is calculated in real time.

22. The memory system according to claim 17 is a flash memory.

23. A memory system comprising:

a plurality of memory groups, each of said memory groups comprising a plurality of memory cells;

a plurality of group tags, each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected; and

wherein any combination of the memory groups can be write protected.

24. The memory system according to Claim 23, wherein the number of memory cells in each memory group is configurable.

25. The memory system according to Claim 23, wherein the corresponding cells in each memory group is calculated in real time.

26. The memory system according to claim 22 is a flash memory.